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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/810,905	03/26/2004	Haowen Bu	TI-36637	9390

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EXAMINER	
STARK, JARRETT J	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 07/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/810,905	BU ET AL.	
	Examiner	Art Unit	
	Jarrett J. Stark	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) *11-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 6/5/2006 have been fully considered but they are not persuasive.

Regarding claim 1, in response to applicant's arguments against the references individually (Bu does not teach "cap annealing"), one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

In regards to the argument that Iwasaki does not teach the method of annealing with the cap layer in place. In Iwasaki, Col.8 lines 15-17

"for this reason, as is shown in FIG. 7, cap annealing is performed instead.", Iwasaki specifically states cap-annealing is preformed and also states a benefit of its use. The citation presented by the Applicant's representative is teaching the disadvantages of "capless" annealing.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re*

Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the use the reference is merely to point out, that it is known in the art to use cap annealing when forming thin film transistor gate stacks. It is notoriously well known in the art that when activating the impurities during the formation of a tft a cap layer during the annealing can optionally be used to increase the electron mobility of the doped regions. Cap annealing is a well documented procedure to used when forming all types of (MOS, MES, or MIS) FETs. Please see additional references listed here and on the 892 form:

Kuroda (US 4,797,371) – Cap-annealing a MOS FET and a MES FET

Simakura et al. (US 5,173,127) – Cap-annealing a MIS FET

Chen et al. (US 5,656,546) – Cap-annealing a MOS FET

Furthermore in response to applicant's arguments, the recitation "a CMOS" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

In regards to claim 6, in which the applicant's representative argues that Bu does not teach forming an interfacial layer of nitrogen by one of the methods listed.

Bu et al. states:

"The silicon oxynitride layer 110 can be formed using SiH.sub.4 or Si.sub.2 H.sub.6, NH.sub.3, and N.sub.2 O in a chemical vapor deposition (CVD) process. In particular at temperatures between 600.degree. C. and 750.degree. C., 2-20 sccm of SiH.sub.4, 50-300 sccm of N.sub.2 O, and 1000-5000 sccm of NH.sub.3 can be used to form the oxynitride layer. This process can be performed in a single wafer heater based or rapid thermal type chamber or a conventional batch furnace." Col 3 lines 42-49)

During the CVD process NH_3 is used at elevated temperatures to form the oxynitride layer, there for it is inherent that there is thermal annealing in involved in the process. Whenever the temperature is raised thermal annealing occurs. The citation also state the process can take place in *"a single wafer heater based or rapid thermal type chamber or a conventional batch furnace."* All the stated locating are used to anneal. Also plasma treatments are commonly performed to assist/enhance CVD.

It is also noted that all the methods of forming a oxynitride listed in claim 6 are notoriously well known in the art and it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a know method of oxynitride formation, since it has been held to be within the general skill of a worker in the art to select a known process on the base of its suitability, for its intended use involves only ordinary skill in the art.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-10 are rejected under 35 U.S.C. 103(a) as being obvious over Bu et al. (US 6,677,201) in view of Iwasaki (US 5,143,856).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

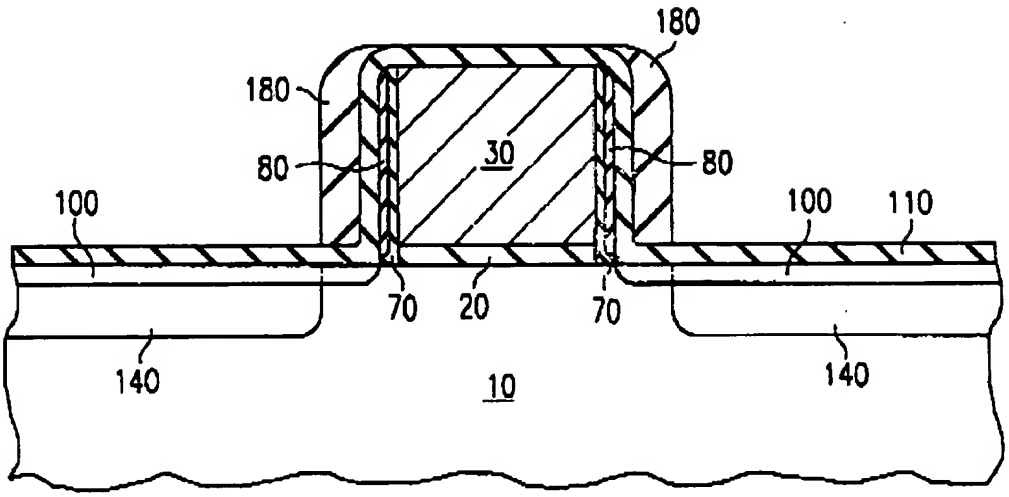

FIG. 4

Regarding claim 1, Bu discloses a method for fabricating a CMOS transistor structure, comprising the steps of: (see Bu, Figs. 2 - 4)

providing a semiconductor substrate having a P-type dopant region to support an N-channel transistor and an N-type dopant region to support a P-channel transistor, each of the N-type dopant and P-type dopant regions having an overlying gate stack including a conductive gate;

forming lightly-doped extension regions in the semiconductor substrate adjacent each gate stack;

forming a layer of insulating material over the lightly-doped extension regions;

forming an interfacial layer of nitrogen at the interface of the insulating layer and the lightly-doped extension regions; forming source and drain regions in the semiconductor substrate adjacent to each of the gate stacks.

Bu does not expressly disclose forming a capping layer of contiguous silicon nitride over the semiconductor substrate and each of the gate stacks;

annealing, with the capping layer in place,

the extension and source and drain regions; and removing the capping layer after the annealing.

Iwasaki discloses the method of cap-annealing with a protective film shown below in Figs 6-7 that can be comprised of several materials including SiN (Iwasaki Col.8 lines 18-25).

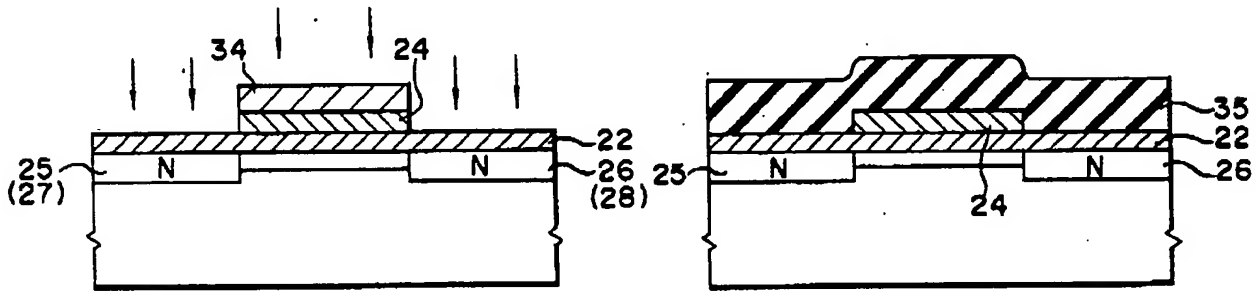

FIG. 6 FIG. 7

The two references are analogous art because they are the same field of endeavor and a similar problem solving area of cap-annealing during the fabrication of a transistor.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include a SiN protective capping layer for use during the annealing step in order to protect the device or layers during the annealing process. Therefore, it would have been obvious to combine Iwasaki with Bu to obtain the invention as specified.

According to Iwasaki Cap-annealing is a safer method than that of capless annealing (Iwasaki, Col.8 lines 15-17). This causes mutual-conductance gm to increase and further improves the operation speed. (Iwasaki, Col.8 lines 8-9).

Regarding claims 2 & 3, Bu in view of Iwasaki discloses the method of claim 1 wherein the extension regions for the PMOS transistors have a dopant concentration in the range of about 1-2 e20 atoms/cm3. (see Bu, Figs. 3)

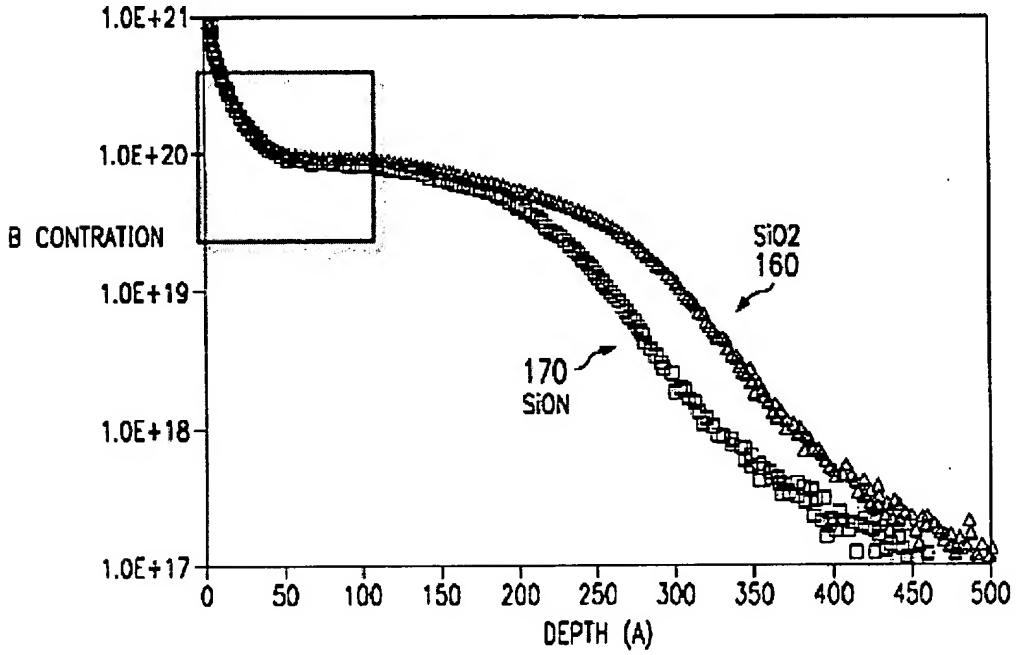

FIG. 3

Regarding claims 4, Bu in view of Iwasaki discloses the method of claim 1 wherein said interfacial nitride layer has an atomic nitrogen concentration in the range of 2-15 atomic percent. (Bu, Col. 2 lines 2-3)

Regarding claims 5, Bu in view of Iwasaki discloses the method of claim 1 wherein the insulting layer is selected from the group comprising silicon nitride and silicon oxide. (Bu, Col. 2 lines 50-67)

Regarding claims 6, Bu in view of Iwasaki discloses the method of claim 1 wherein the step of forming an interfacial layer of nitrogen is performed using one of the methods selected from the group comprising an NH.sub.3 thermal annealing (Bu, Col. 3 line 49 -- RTA) , an NH.sub.3 or N.sub.2 plasma treatment (CVD at the temp. range disclosed by Bu is a form of plasma deposition). (Bu, Col. 3 lines 43-47)

Regarding claims 7, Bu in view of Iwasaki discloses the method of claim 1 wherein the capping layer has a thickness in the range of 200-1000 angstroms.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value for the thickness through routine experimentation and optimization to obtain optimal or desired device performance because the thickness is a result-effective variable and there is no evidence indicating that it is critical or produces any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05

Given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved. See In re Aller, Lacey and Hall (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation." Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant

must show that the chosen dimensions are critical. In re Woodruff, 919 f.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Any differences in the claimed invention and the prior art may be expected to result in some differences in properties. The issue is whether the properties differ to such an extent that the difference is really unexpected. In re Merck & Co., 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Appellants have the burden of explaining the data in any declaration they proffer as evidence of non-obviousness. Ex parte Ishizaka, 24 USPQ2d 1621, 1624 (Bd. Pat. App. & Inter. 1992).

An Affidavit or declaration under 37 CFR 1.132 must compare the claimed subject matter with the closest prior art to be effective to rebut a prima facie case of obviousness. In re Burckel, 592 F.2d 1175, 201 USPQ 67 (CCPA 1979).

Regarding claims 8, Bu in view of Iwasaki discloses the method of claim 1 wherein the annealing step is performed in the range of 1000-1100 degrees centigrade for a time in the range of less than about 10 seconds. (Bu, Col. 3 line 29) – Typical ranges for RTA

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value for the temperature and time through routine experimentation and optimization to obtain optimal or desired device performance because the temperature and time is a result-effective variable and there is no evidence indicating that it is critical or produces any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05

Regarding claims 9, Bu in view of Iwasaki discloses the method of claim 1 wherein said gate stack further includes a nitride sidewall deposited with a BTBAS precursor. (Bu, Col. 3 line 54)

Regarding claims 10, Bu in view of Iwasaki discloses a method for fabricating a CMOS transistor structure, comprising the steps of: providing a semiconductor substrate having an N-type dopant region to support an PMOS transistor and a P-type dopant region to support a NMOS transistor, each of the N-type dopant and P-type dopant regions having an overlying gate stack including a conductive gate; forming lightly-doped extension regions in the semiconductor substrate adjacent each gate stack, the lightly-doped extension regions in the N-type dopant region comprising a P-type dopant having a dopant concentration in the range of about 1-2 e20 atoms/cm3; forming a layer of silicon oxide over the lightly-doped extension regions; forming an interfacial layer of nitrogen between the lightly-doped extension regions and the silicon oxide layer, the interfacial layer of nitrogen having an atomic nitrogen concentration in the range of 2-15 atomic percent; forming source and drain regions in the semiconductor substrate adjacent to each of the gate stacks, the source and drain regions in the in the N-type dopant region comprising a P-type dopant having a concentration in the range of about 1-2 e20 atoms/cm3; forming a capping layer of contiguous silicon nitride having a thickness in the range of about 200-1000 angstroms over the semiconductor substrate and each of the gate stacks; annealing, with the capping layer in place, the extension and source and drain regions at a temperature in

the range of 1000-1100 degrees centigrade for a period in the range of less than about 10 seconds; and removing the nitride cap after the annealing. (See above regarding claims 1-9)

Conclusion

If applicants desire to further prosecution, it is highly suggested that applicants closely consider, Sayama et al. (US 2004/0097030). Sayama et al. discloses in detail the effects and benefits of the induced stress during the cap-annealing step.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jarrett J. Stark whose telephone number is (571) 272-6005. The examiner can normally be reached on Monday - Thursday 7:00AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JJS
June 26, 2006

MICHELLE ESTRADA
PRIMARY EXAMINER